MC34261, MC33261

Power Factor Controllers

The MC34261/MC33261 are active power factor controllers specifically designed for use as a preconverter in electronic ballast and in off−line power converter applications. These integrated circuits feature an internal startup timer, a one quadrant multiplier for near unity power factor, zero current detector to ensure critical conduction operation, high gain error amplifier, trimmed internal bandgap reference, current sensing comparator, and a totem pole output ideally suited for driving a power MOSFET.

Also included are protective features consisting of input undervoltage lockout with hysteresis, cycle−by−cycle current limiting, and a latch for single pulse metering. These devices are available in dual−in−line and surface mount plastic packages.

- Internal Startup Timer
- One Quadrant Multiplier
- Zero Current Detector
- Trimmed 2% Internal Bandgap Reference
- Totem Pole Output
- Undervoltage Lockout with Hysteresis
- Low Startup and Operating Current
- Pinout Equivalent to the SG3561
- Functional Equivalent to the TDA4817

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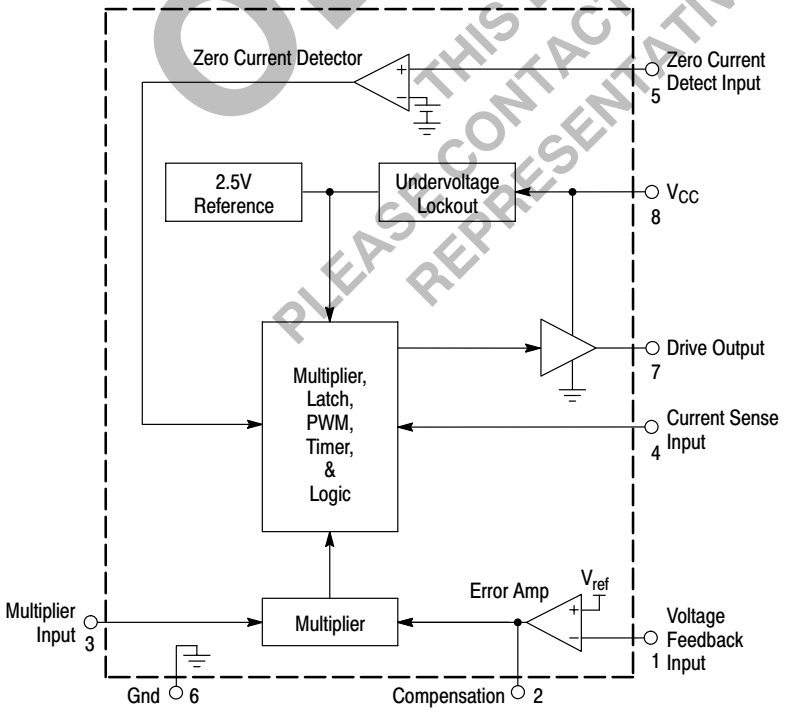
Simplified Block Diagram



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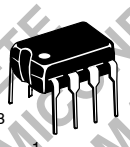
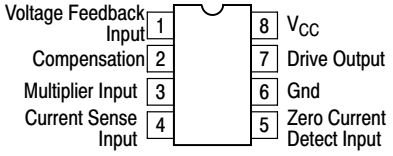
POWER FACTOR CONTROLLERS SEMICONDUCTOR TECHNICAL DATA



P SUFFIX
PLASTIC PACKAGE
CASE 626

D SUFFIX
PLASTIC PACKAGE
CASE 751
(SO−8)

PIN CONNECTIONS



(Top View)

ORDERING INFORMATION

Device	Operating Temperature Range	Package
MC34261D	T_A = 0° to +70°C	SO−8
MC34261P		Plastic DIP
MC33261D	T_A = −40° to +85°C	SO−8
MC33261P		Plastic DIP

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MAXIMUM RATINGS

Rating	Symbol	Value	Unit
Total Power Supply and Zener Current	$(I_{CC} + I_Z)$	30	mA
Output Current, Source or Sink (Note 1)	I_O	500	mA
Current Sense, Multiplier, and Voltage Feedback Inputs	V_{in}	−1.0 to 10	V
Zero Current Detect Input High State Forward Current Low State Reverse Current	I_{in}	 50 −10	mA
Power Dissipation and Thermal Characteristics P Suffix, Plastic Package Case 626 Maximum Power Dissipation @ T_A = 70°C Thermal Resistance, Junction−to−Air D Suffix, Plastic Package Case 626 Maximum Power Dissipation @ T_A = 70°C Thermal Resistance, Junction−to−Air	 P_D $R_{\theta JA}$ P_D $R_{\theta JA}$	 800 100 450 178	 mW °C/W mW °C/W
Operating Junction Temperature	T_J	+150	°C
Operating Ambient Temperature (Note 3) MC34261 MC33261	T_A	 0 to +70 −40 to +85	°C
Storage Temperature	T_{stg}	−55 to +150	°C

ELECTRICAL CHARACTERISTICS (V_{CC} = 12 V, for typical values T_A = 25°C, for min/max values T_A is the operating ambient temperature range that applies [Note 3], unless otherwise noted.)

Characteristic	Symbol	Min	Typ	Max	Unit
ERROR AMPLIFIER					
Voltage Feedback Input Threshold T_A = 25°C $T_A = T_{low}$ to T_{high} (V_{CC} = 12 V to 28 V)	V_{FB}	 2.465 2.44	2.5	 2.535 2.54	V
Line Regulation (V_{CC} = 12 V to 28 V, T_A = 25°C)	Reg_{line}	–	1.0	10	mV
Input Bias Current (V_{FB} = 0 V)	I_{IB}	–	−0.3	−1.0	μA
Open Loop Voltage Gain	A_{VOL}	65	85	–	dB
Gain Bandwidth Product (T_A = 25°C)	GBW	0.7	1.0	–	MHz
Output Source Current (V_O = 4.0 V, V_{FB} = 2.3 V)	I_{Source}	0.25	0.5	0.75	mA
Output Voltage Swing High State (I_{Source} = 0.2 mA, V_{FB} = 2.3 V) Low State (I_{Sink} = 0.4 mA, V_{FB} = 2.7 V)	 V_{OH} V_{OL}	 5.0 –	 5.7 2.1	 – 2.44	V
MULTIPLIER					
Dynamic Input Voltage Range Multiplier Input (Pin 3) Compensation (Pin 2)	 $V_{Pin\ 3}$ $V_{Pin\ 2}$	 0 to 2.5 V_{FB} to (V_{FB} + 1.0)	 0 to 3.5 V_{FB} to (V_{FB} + 1.5)	 – –	V
Input Bias Current (V_{FB} = 0 V)	I_{IB}	–	−0.3	−1.0	μA
Multiplier Gain ($V_{Pin\ 3}$ = 0.5 V, $V_{Pin\ 2} = V_{FB}$ + 1.0 V) (Note 2)	K	0.4	0.62	0.8	1/V
ZERO CURRENT DETECTOR					
Input Threshold Voltage (V_{in} Increasing)	V_{th}	1.3	1.6	1.8	V
Hysteresis (V_{in} Decreasing)	V_H	40	110	200	mV
Input Clamp Voltage High State (I_{DET} = 3.0 mA) Low State (I_{DET} = −3.0 mA)	 V_{IH} V_{IL}	 6.1 0.3	 6.7 0.7	 – 1.0	V

NOTES: 1. Maximum package power dissipation limits must be observed.

2. $K = \dfrac{\text{Pin 4 Threshold Voltage}}{V_{Pin\ 3}(V_{Pin\ 2} - V_{FB})}$

3. T_{low} = 0°C for MC34261 = −40°C for MC33261 T_{high} = +70°C for MC34261 = +85°C for MC33261

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ELECTRICAL CHARACTERISTICS (V_{CC} = 12 V, for typical values T_A = 25°C, for min/max values T_A is the operating ambient temperature range that applies [Note 3], unless otherwise noted.)

Characteristic	Symbol	Min	Typ	Max	Unit
CURRENT SENSE COMPARATOR					
Input Bias Current ($V_{Pin\ 4}$ = 0 V)	I_{IB}	–	–0.5	–2.0	μA
Input Offset Voltage ($V_{Pin\ 2}$ = 1.1 V, $V_{Pin\ 3}$ = 0 V)	V_{IO}	–	3.5	15	mV
Delay to Output	$t_{PHL\ (in/out)}$	–	200	400	ns
DRIVE OUTPUT					
Output Voltage (V_{CC} = 12 V) Low State (I_{Sink} = 20 mA) (I_{Sink} = 200 mA) High State (I_{Source} = 20 mA) (I_{Source} = 200 mA)	 V_{OL} V_{OH} 	 – 1.8 9.8 7.8	 0.3 2.4 10.3 8.3	 0.8 3.3 – 8.8	V
Output Voltage (V_{CC} = 30 V) High State (I_{Source} = 20 mA, C_L = 15 pF)	$V_{O(max)}$	14	16	18	V
Output Voltage Rise Time (C_L = 1.0 nF)	t_r	–	50	120	ns
Output Voltage Fall Time (C_L = 1.0 nF)	t_f	–	50	120	ns
Output Voltage with UVLO Activated (V_{CC} = 7.0 V, I_{Sink} = 1.0 mA)	$V_{OH(UVLO)}$	–	0.2	0.8	V
RESTART TIMER					
Restart Time Delay	t_{DLY}	150	400	–	μs
UNDERVOLTAGE LOCKOUT					
Startup Threshold (V_{CC} Increasing)	V_{th}	9.2	10.0	10.8	V
Minimum Operating Voltage After Turn–On (V_{CC} Decreasing)	$V_{Shutdown}$	7.0	8.0	9.0	V
Hysteresis	V_H	1.75	2.0	2.5	V
TOTAL DEVICE					
Power Supply Current Startup (V_{CC} = 7.0 V) Operating Dynamic Operating (50 kHz, C_L = 1.0 nF)	I_{CC} 	 – – –	 0.3 7.1 9.0	 0.5 12 20	mA
Power Supply Zener Voltage	V_Z	30	36	–	V

NOTES: 1. Maximum package power dissipation limits must be observed.

2. $K = \dfrac{\text{Pin 4 Threshold Voltage}}{V_{Pin\ 3}(V_{Pin\ 2} - V_{FB})}$

3. T_{low} = 0°C for MC34261, −40°C for MC33261 $\quad T_{high}$ = +70°C for MC34261, +85°C for MC33261

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Figure 1. Current Sense Input Threshold versus Multiplier Input

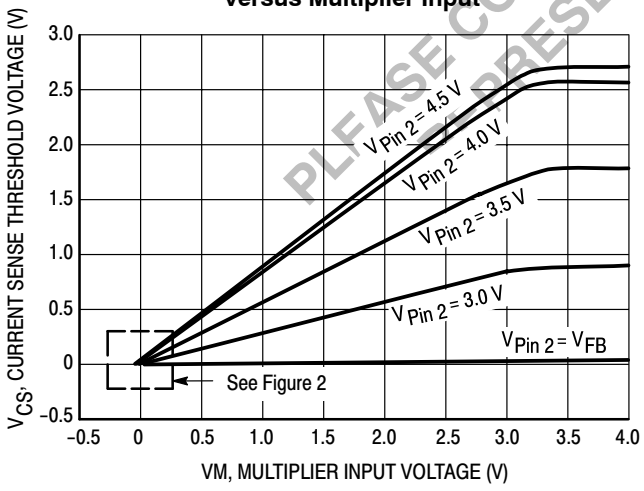

Figure 2. Current Sense Input Threshold versus Multiplier Input

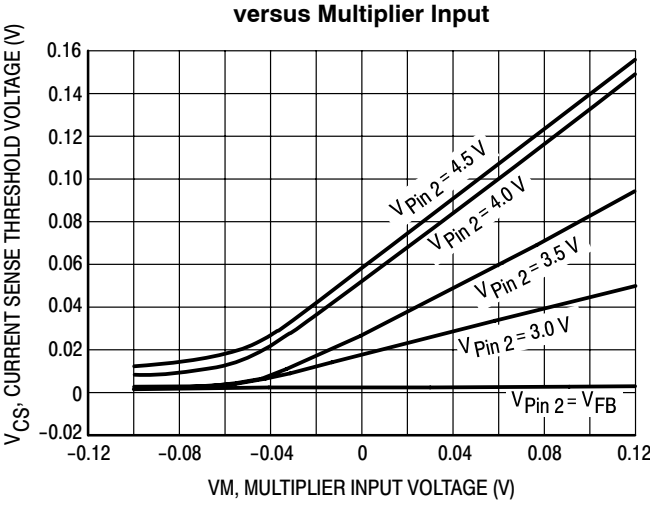

Figure 3. Voltage Feedback Input Threshold Change versus Temperature

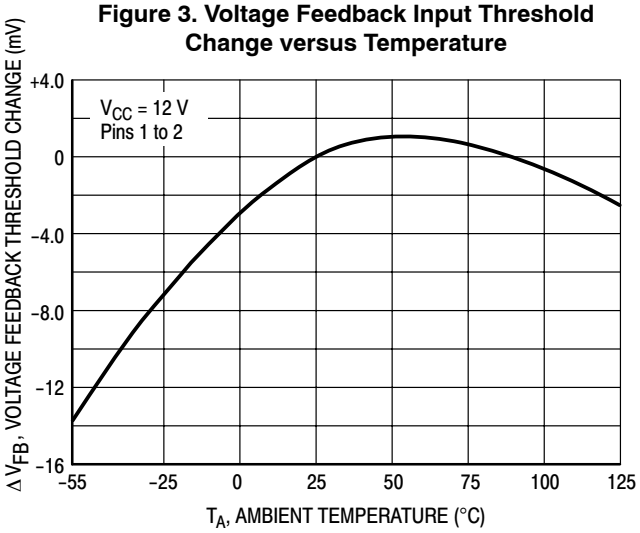

Figure 4. Error Amp Open Loop Gain and Phase versus Frequency

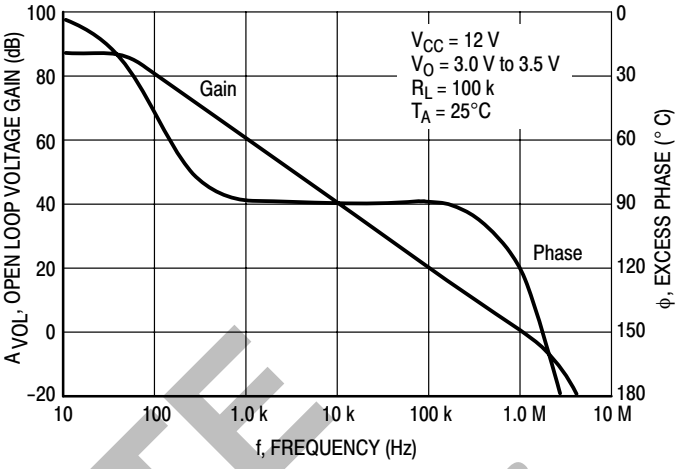

Figure 5. Error Amp Small Signal Transient Response

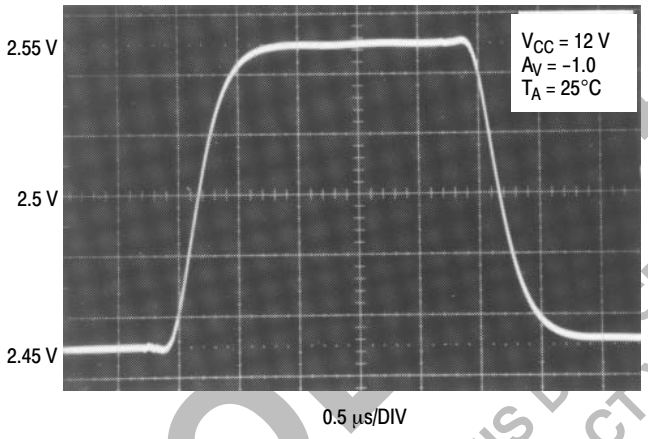

Figure 6. Error Amp Large Signal Transient Response

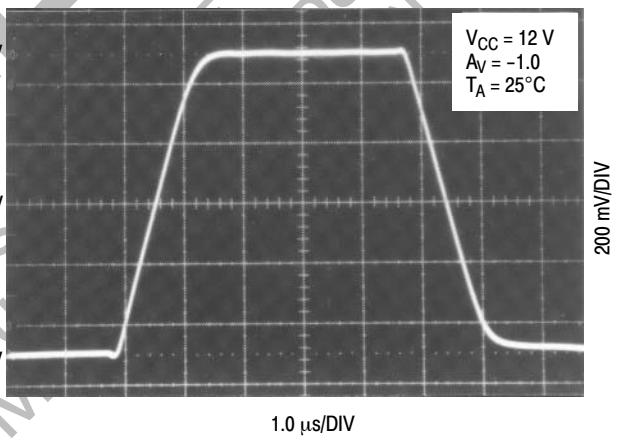

Figure 7. Error Amp Output Saturation versus Sink Current

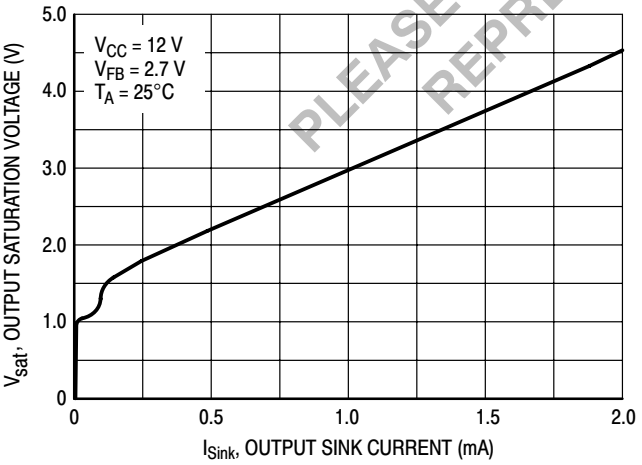

Figure 8. Restart Time Delay versus Temperature

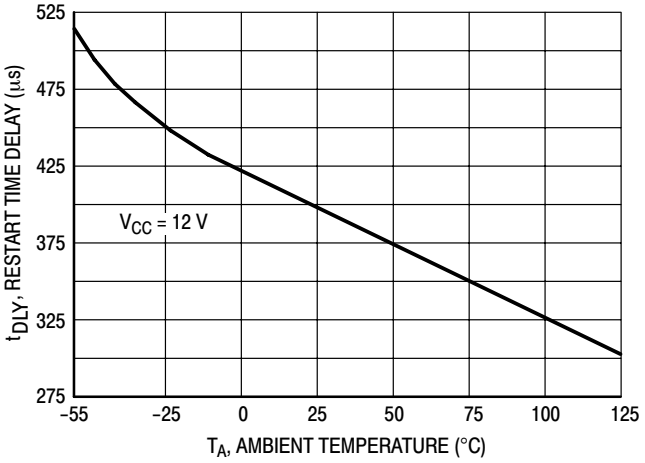

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Figure 9. Zero Current Detector Input Threshold Voltage Change versus Temperature

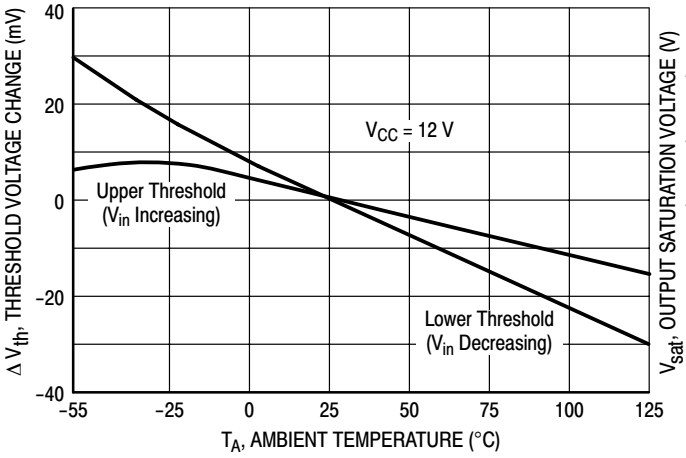


Figure 10. Output Saturation Voltage versus Load Current

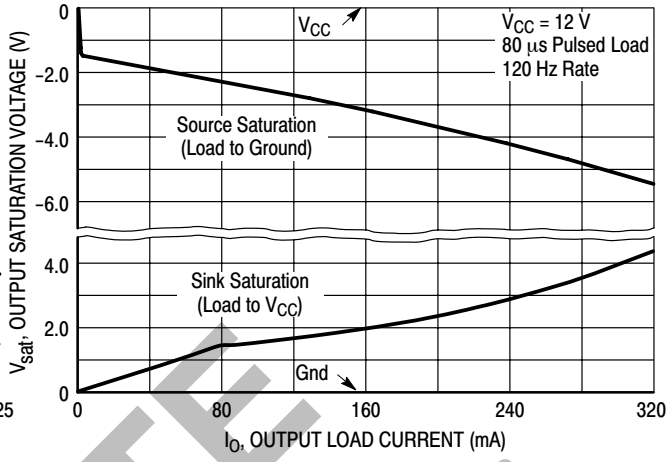


Figure 11. Drive Output Waveform

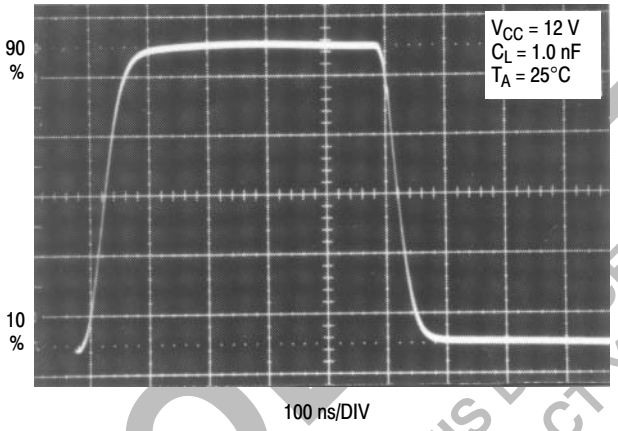


Figure 12. Drive Output Cross Conduction

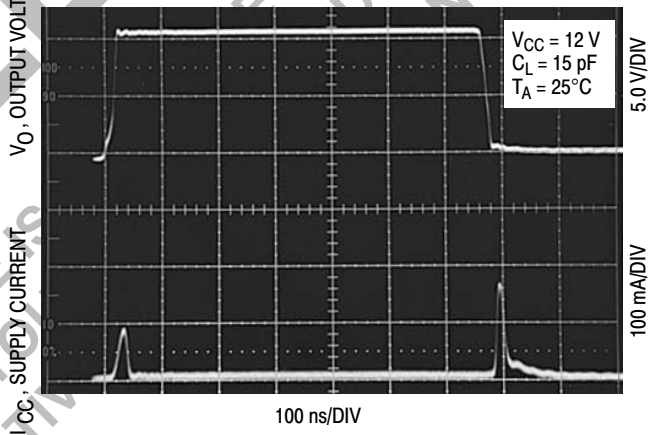


Figure 13. Supply Current versus Supply Voltage

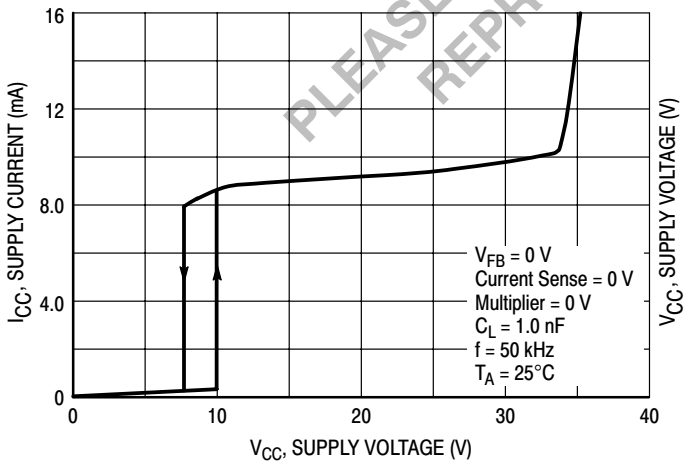
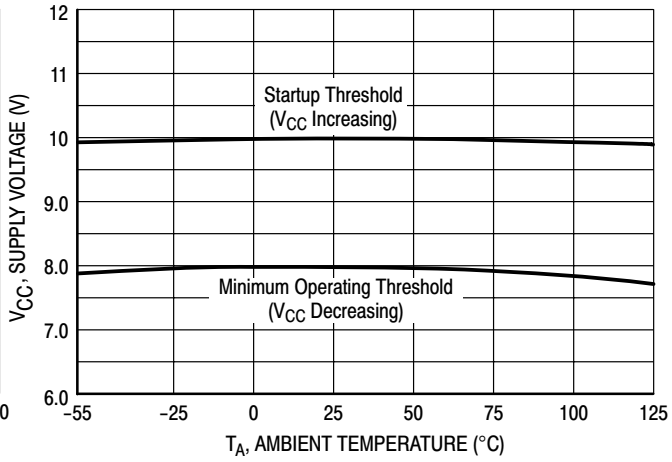


Figure 14. Undervoltage Lockout Thresholds versus Temperature



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FUNCTIONAL DESCRIPTION

Introduction

Most electronic ballasts and switching power supplies use a bridge rectifier and a filter capacitor to derive raw dc voltage from the utility ac line. This simple rectifying circuit draws power from the line when the instantaneous ac voltage exceeds the capacitor's voltage. This occurs near the line voltage peak and results in a high charge current spike. Since power is only taken near the line voltage peaks, the resulting spikes of current are extremely nonsinusoidal with a high content of harmonics. This results in a poor power factor condition where the apparent input power is much higher than the real power.

The MC34261, MC33261 are high performance, critical conduction, current mode power factor controllers specifically designed for use in off−line active preconverters. These devices provide the necessary features required to significantly enhance poor power factor loads by keeping the ac line current sinusoidal and in phase with the line voltage. With proper control of the preconverter, almost any complex load can be made to appear resistive to the ac line, thus significantly reducing the harmonic current content.

Operating Description

The MC34261, MC33261 contains many of the building blocks and protection features that are employed in modern high performance current mode power supply controllers. There are, however, two areas where there is a major difference when compared to popular devices such as the UC3842 series. Referring to the block diagram in Figure 15, note that a multiplier has been added to the current sense loop and that this device does not contain an oscillator. A description of each of the functional blocks is given below.

Error Amplifier

A fully compensated Error Amplifier with access to the inverting input and output is provided. It features a typical dc voltage gain of 85 dB, and a unity gain bandwidth of 1.0 MHz with 58° of phase margin (Figure 4). The noninverting input is internally biased at 2.5 V ±2.0% and is not pinned out. The output voltage of the power factor converter is typically divided down and monitored by the inverting input. The maximum input bias current is −1.0 μA which can cause an output voltage error that is equal to the product of the input bias current and the value of the upper divider resistor R_2. The Error Amp Output is internally connected to the Multiplier and is pinned out (Pin 2) for external loop compensation. Typically, the bandwidth is set below 20 Hz, so that the Error Amp output voltage is relatively constant over a given ac line cycle. The output stage consists of a 500 μA current source pull−up with a Darlington transistor pull−down. It is capable of swinging from 2.1 V to 5.7 V, assuring that the Multiplier can be driven over its entire dynamic range.

Multiplier

A single quadrant, two input multiplier is the critical element that enables this device to control power factor. The ac haversines are monitored at Pin 3 with respect to ground while the Error Amp output at Pin 2 is monitored with respect to the Voltage Feedback Input threshold. A graph of the Multiplier transfer curve is shown in Figure 1. Note that both inputs are extremely linear over a wide dynamic range, 0 V to 3.2 V for the Multiplier input (Pin 3), and 2.5 V to 4.0 V for the Error Amp output (Pin 2). The Multiplier output controls the Current Sense Comparator threshold (Pin 4) as the ac voltage traverses sinusoidally from zero to peak line. This has the effect of forcing the MOSFET peak current to track the input line voltage, thus making the preconverter load appear to be resistive.

$$\text{Pin 4 Threshold} \approx 0.62(V_{\text{Pin 2}} - V_{FB})V_{\text{Pin 3}}$$

Zero Current Detector

The MC34261 operates as a critical conduction current mode controller, whereby output switch conduction is initiated by the Zero Current Detector and terminated when the peak inductor current reaches the threshold level established by the Multiplier output. The Zero Current Detector initiates the next on−time by setting the RS Latch at the instant the inductor current reaches zero. This critical conduction mode of operation has two significant benefits. First, since the MOSFET cannot turn on until the inductor current reaches zero, the output rectifier's reverse recovery time becomes less critical allowing the use of an inexpensive rectifier. Second, since there are no deadtime gaps between cycles, the ac line current is continuous thus limiting the peak switch to twice the average input current.

The Zero Current Detector indirectly senses the inductor current by monitoring when the auxiliary winding voltage falls below 1.6 V. To prevent false tripping, 110 mV of hysteresis is provided. The Zero Current Detector input is internally protected by two clamps. The upper 6.7 V clamp prevents input overvoltage breakdown while the lower 0.7 V clamp prevents substrate injection. Device destruction can result if this input is shorted to ground. An external resistor must be used in series with the auxiliary winding to limit the current through the clamps.

Current Sense Comparator and RS Latch

The Current Sense Comparator RS Latch configuration ensures that only a single pulse appears at the Drive Output during a given cycle. The inductor current is converted to a voltage by inserting a ground referenced sense resistor R_9 in series with the source of output switch Q1. This voltage is monitored by the Current Sense Input and compared to the Multiplier output voltage. The peak inductor current is controlled by the threshold voltage of Pin 4 where:

$$I_{pk} = \frac{\text{Pin 4 Threshold}}{R_9}$$

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With the component values shown in Figure 16, the Current Sense Comparator threshold, at the peak of the haversine varies from 1.1 V at 90 Vac to 100 mV at 268 Vac. The Current Sense Input to Drive Output propagation delay is typically 200 ns.

Timer

A watchdog timer function was added to the IC to eliminate the need for an external oscillator when used in stand alone applications. The Timer provides a means to automatically start or restart the preconverter if the Drive Output has been off for more than 400 μs after the inductor current reaches zero.

Undervoltage Lockout

An Undervoltage Lockout comparator guarantees that the IC is fully functional before enabling the output stage. The positive power supply terminal (V_{CC}) is monitored by the UVLO comparator with the upper threshold set at 10 V and the lower threshold at 8.0 V (Figure 14). In the standby mode, with V_{CC} at 7.0 V, the required supply current is less than 0.5 mA (Figure 13). This hysteresis and low startup current allow the implementation of efficient bootstrap startup techniques, making these devices ideally suited for wide input range off line preconverter applications. An internal 36 V clamp has been added from V_{CC} to ground to protect the IC and capacitor C_5 from an overvoltage condition. This feature is desirable if external circuitry is used to delay the startup of the preconverter.

Output

The MC34261/MC33261 contain a single totem pole output stage specifically designed for direct drive of power MOSFETs. The Drive Output is capable of up to ±500 mA peak current with a typical rise and fall time of 50 ns with a 1.0 nF load. Additional internal circuitry has been added to keep the Drive Output in a sinking mode whenever the Undervoltage Lockout is active. This characteristic eliminates the need for an external gate pull−down resistor. The totem pole output has been optimized to minimize cross conduction current during high speed operation. The addition of two 10 Ω resistors, one in series with the source output transistor and one in series with the sink output transistor, reduces the cross conduction current, as shown in Figure 12. A 16 V clamp has been incorporated into the output stage to limit the high state V_{OH}. This prevents rupture of the MOSFET gate when V_{CC} exceeds 20 V.

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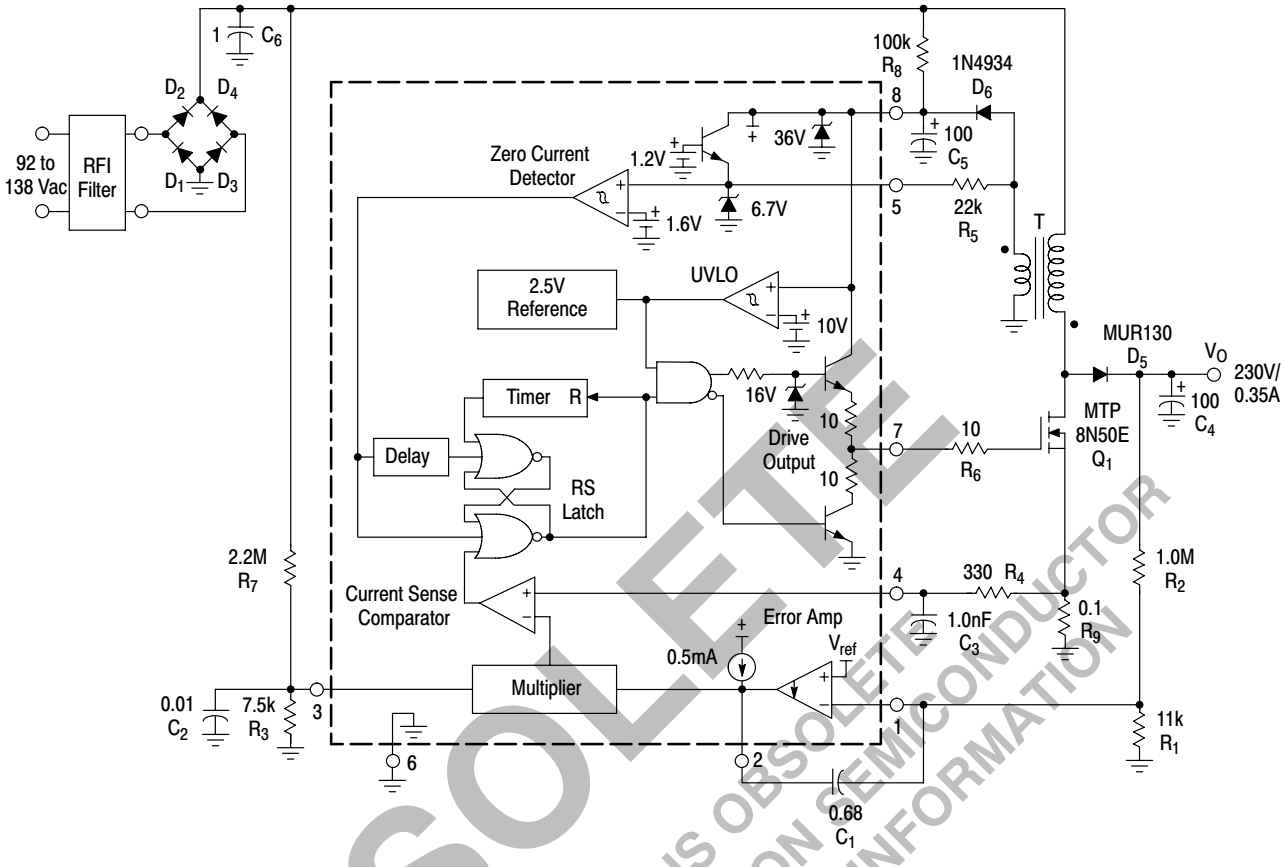
Table 1. Design Equations

Notes	Calculation	Formula
Calculate the maximum required output power.	Required Converter Output Power	$P_O = V_O I_O$
Calculated at the minimum required ac line for regulation. Let the efficiency n = 0.95.	Peak Inductor Current	$I_{L(pk)} = \frac{2\sqrt{2}\,P_O}{\eta Vac_{(LL)}}$
Let the switching cycle t = 20 μs.	Inductance	$L = \frac{2t\left(\frac{V_O}{\sqrt{2}} - Vac\right) Vac^2}{V_O\, Vac_{(LL)}\, I_{L(pk)}}$
In theory the on−time t_{on} is constant. In practice t_{on} tends to increase at the ac line zero crossings due to the charge on capacitor C_6.	Switch On−Time	$t_{on} = \frac{2\,P_O\,L}{\eta\, Vac^2}$
The off−time t_{off} is greatest at peak ac line and approaches zero at the ac line zero crossings. Theta (θ) represents the angle of the ac line voltage.	Switch Off−Time	$t_{off} = \frac{t_{on}}{\frac{V_O}{\sqrt{2}\,Vac\,\lvert Sin\,\theta\rvert}} - 1$
The minimum switching frequency occurs at peak ac line and increases as t_{off} decreases.	Switching Frequency	$f = \frac{1}{t_{on} + t_{off}}$
Set the current sense threshold V_{CS} to 1.0 V for universal input (85 Vac to 265 Vac) operation and to 0.5 V for fixed input (92 Vac to 138 Vac, or 184 to 276 Vac) operation.	Peak Switch Current	$R_9 = \frac{V_{CS}}{I_{L(pk)}}$
Set the multiplier input voltage V_M to 3.0 V at high line. Empirically adjust V_M for the lowest distortion over the ac line range while guaranteeing startup at minimum line.	Multiplier Input Voltage	$V_M = \frac{Vac\,\sqrt{2}}{\left(\frac{R_7}{R_3} + 1\right)}$
The $I_{IB}\,R_1$ error term can be minimized with a divider current in excess of 100 μA.	Converter Output Voltage	$V_O = V_{ref}\left(\frac{R_2}{R_1} + 1\right) - I_{IB}\,R_2$
The bandwidth is typically set to 20 Hz for minimum output ripple over the ac line haversine.	Error Amplifier Bandwidth	$BW = \frac{1}{2\pi\frac{R_1 R_2}{R_1 + R_2} C_1}$

The following converter characteristics must be chosen:

V_O − Desired output voltage
I_O − Desired output current
Vac − AC RMS line voltage
$Vac_{(LL)}$ − AC RMS low line voltage

Figure 15. 80 W Power Factor Controller



Power Factor Controller Test Data

AC Line Input								DC Output				
			Current Harmonic Distortion (%)									
V_{rms}	P_{in}	PF	THD	2	3	5	7	$V_{O(pp)}$	V_O	I_O	P_O	n(%)
90	85.6	−0.998	2.4	0.11	0.52	1.3	0.67	10.0	230	0.350	80.5	94.0
100	85.1	−0.997	5.0	0.13	1.7	2.4	1.4	10.1	230	0.350	80.5	94.6
110	84.8	−0.997	5.3	0.12	2.5	2.6	1.5	10.2	230	0.350	80.5	94.9
120	84.5	−0.997	5.8	0.12	3.2	2.7	1.4	10.2	230	0.350	80.5	95.3
130	84.2	−0.996	6.6	0.12	4.0	2.8	1.5	10.2	230	0.350	80.5	95.6
138	84.1	−0.995	7.2	0.13	4.5	3.0	1.6	10.2	230	0.350	80.5	95.7

This data was taken with the test set−up shown in Figure 17.

T = Coilcraft N2881−A
Primary: 62 turns of # 22 AWG
Secondary: 5 turns of # 22 AWG
Core: Coilcraft PT2510, EE 25
Gap: 0.072″ total for a primary inductance of 320 μH

Heatsink = AAVID Engineering Inc. 5903B, or 5930B

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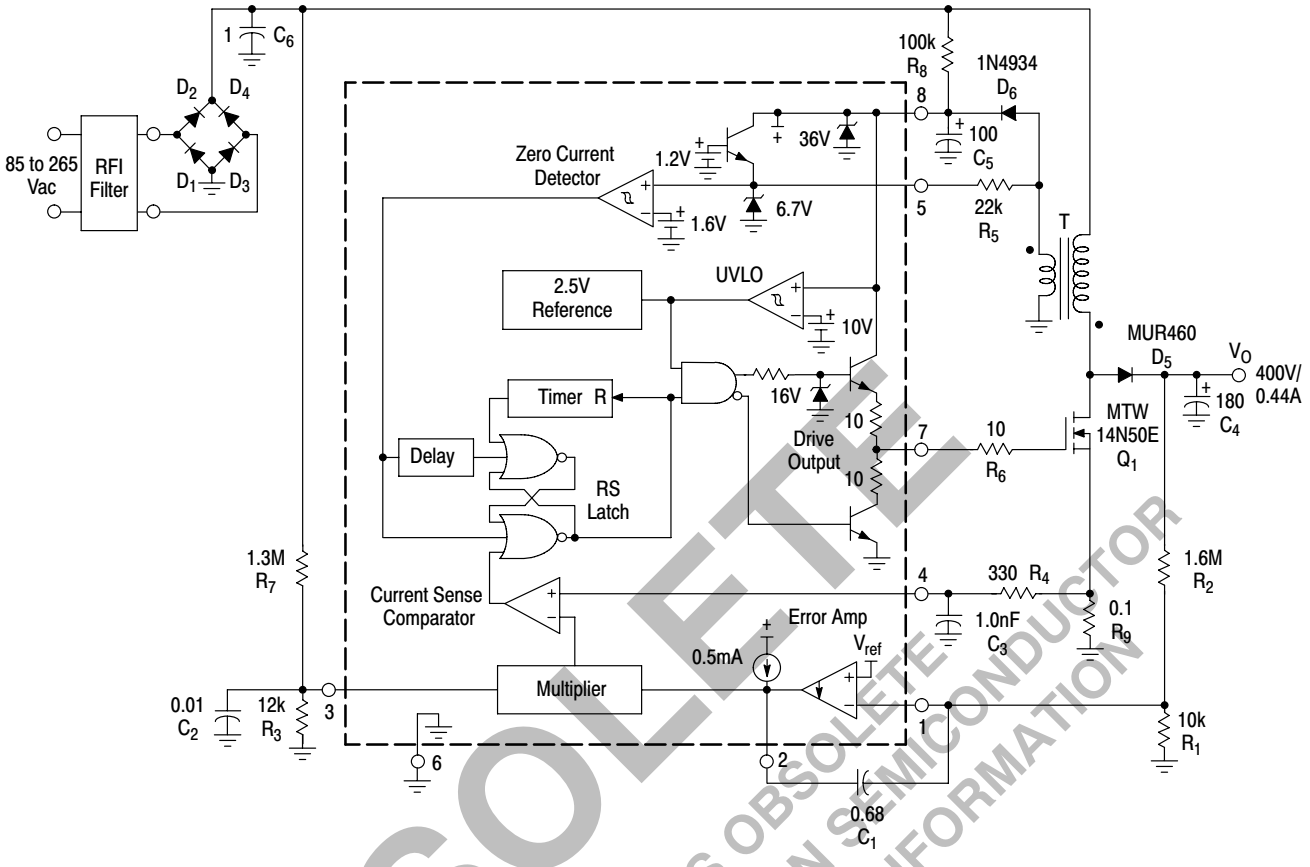
Figure 16. 175 W Universal Input Power Factor Controller



Power Factor Controller Test Data

AC Line Input								DC Output			
			Current Harmonic Distortion (%)								
V_{rms}	P_{in}	PF	THD	2	3	5	7	$V_{O(pp)}$	V_O	I_O	P_O	n(%)
90	187.5	−0.998	2.0	0.10	0.98	0.90	0.78	8.0	400.7	0.436	174.7	93.2
120	184.6	−0.997	1.8	0.09	1.3	1.3	0.93	8.0	400.7	0.436	174.7	94.6
138	183.6	−0.997	2.3	0.05	1.6	1.5	1.0	8.0	400.7	0.436	174.7	95.2
180	181.0	−0.995	4.3	0.16	2.5	2.0	1.2	8.0	400.6	0.436	174.7	95.6
240	179.3	−0.993	6.0	0.08	3.7	2.7	1.4	8.0	400.6	0.436	174.7	97.4
268	178.6	−0.992	6.7	0.16	2.8	3.7	1.7	8.0	400.6	0.436	174.7	97.8

This data was taken with the test set−up shown in Figure 17.

T = Coilcraft N2880−A
Primary: 78 turns of # 16 AWG
Secondary: 6 turns of # 18 AWG
Core: Coilcraft PT4215, EE 42−15
Gap: 0.104″ total for a primary inductance of 870 μH

Heatsink = AAVID Engineering Inc. 5903B

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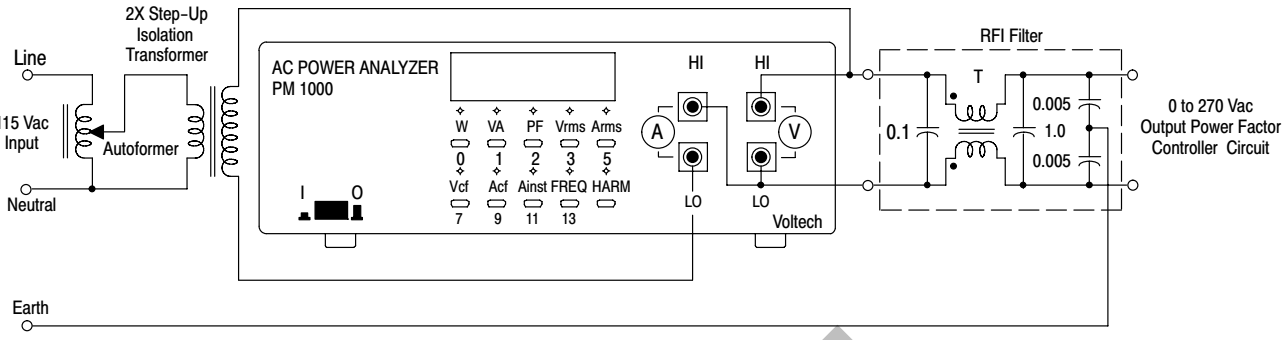
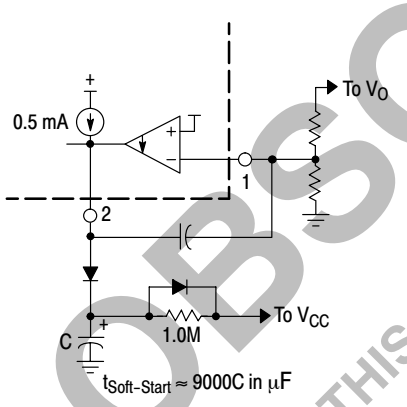
Figure 17. Power Factor Test Set−Up



An RFI filter is required for best performance when connecting the preconverter directly to the AC line. Commercially available two stage filters such as the Delta Electronics 03DPCG5 work excellent. The simple single stage test filter shown above can easily be constructed with a common mode transformer. Transformer (T) is a Coilcraft CMT3−28−2 with 28 mH minimum inductance and a 2.0 A maximum current rating.

Figure 18. Soft−Start Circuit



Startup overshoot can be eliminated with the addition of a Soft−Start circuit.

Figure 19. Error Amp Compensation

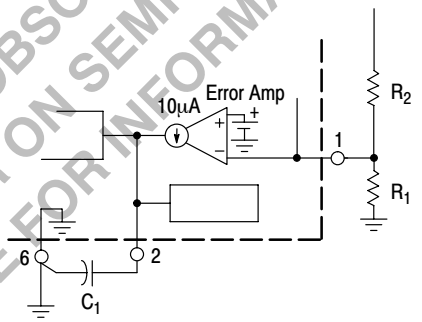


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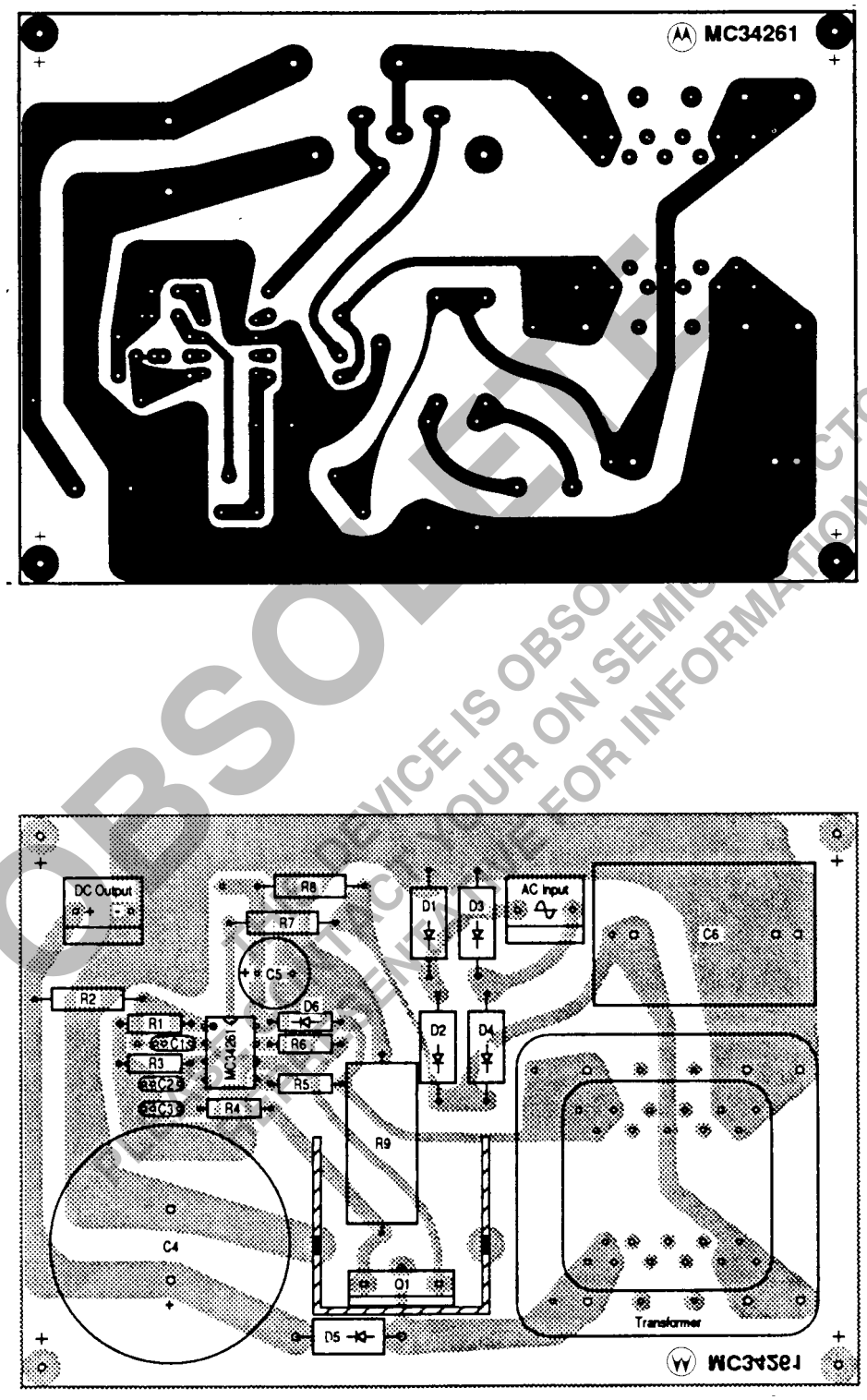
Figure 20. Printed Circuit Board and Component Layout
(Circuits of Figures 15 and 16)



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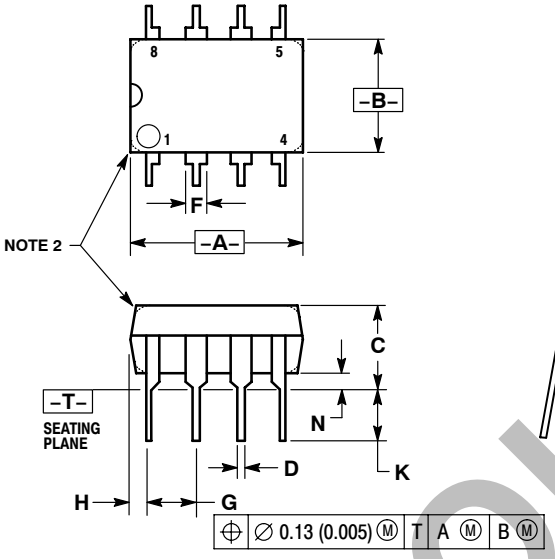
OUTLINE DIMENSIONS

P SUFFIX
PLASTIC PACKAGE
CASE 626−05
ISSUE L



NOTES:
1. DIMENSION L TO CENTER OF LEAD WHEN FORMED PARALLEL.
2. PACKAGE CONTOUR OPTIONAL (ROUND OR SQUARE CORNERS).
3. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.

	MILLIMETERS		INCHES	
DIM	MIN	MAX	MIN	MAX
A	9.40	10.16	0.370	0.400
B	6.10	6.60	0.240	0.260
C	3.94	4.45	0.155	0.175
D	0.38	0.51	0.015	0.020
F	1.02	1.78	0.040	0.070
G	2.54 BSC		0.100 BSC	
H	0.76	1.27	0.030	0.050
J	0.20	0.30	0.008	0.012
K	2.92	3.43	0.115	0.135
L	7.62 BSC		0.300 BSC	
M	---	10°	---	10°
N	0.76	1.01	0.030	0.040

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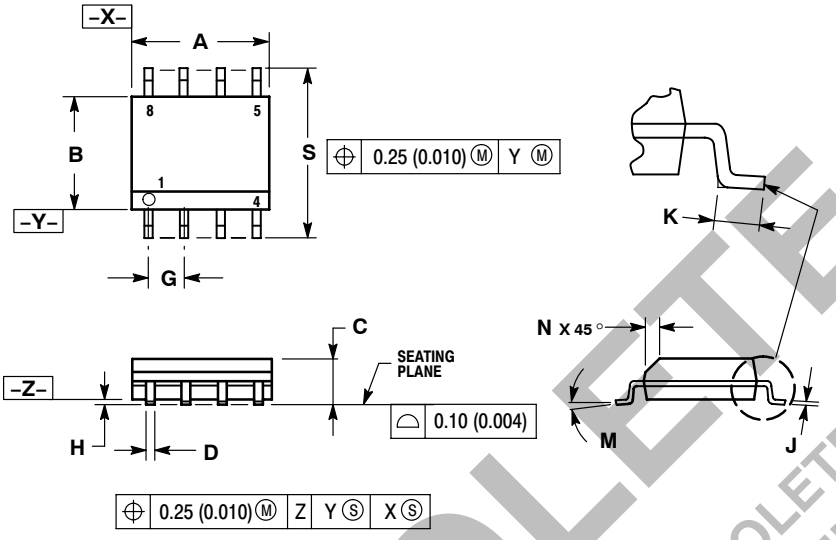
OUTLINE DIMENSIONS

D SUFFIX
PLASTIC PACKAGE
CASE 751−07
(SO−8)
ISSUE W



NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: MILLIMETER.
3. DIMENSION A AND B DO NOT INCLUDE MOLD PROTRUSION.
4. MAXIMUM MOLD PROTRUSION 0.15 (0.006) PER SIDE.
5. DIMENSION D DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL BE 0.127 (0.005) TOTAL IN EXCESS OF THE D DIMENSION AT MAXIMUM MATERIAL CONDITION.

	MILLIMETERS		INCHES	
DIM	MIN	MAX	MIN	MAX
A	4.80	5.00	0.189	0.197
B	3.80	4.00	0.150	0.157
C	1.35	1.75	0.053	0.069
D	0.33	0.51	0.013	0.020
G	1.27 BSC		0.050 BSC	
H	0.10	0.25	0.004	0.010
J	0.19	0.25	0.007	0.010
K	0.40	1.27	0.016	0.050
M	0 °	8 °	0 °	8 °
N	0.25	0.50	0.010	0.020
S	5.80	6.20	0.228	0.244

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